



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,297	01/22/2002	Heinz Walter	740116-358	4774
22204	7590	09/09/2005	EXAMINER	
NIXON PEABODY, LLP 401 9TH STREET, NW SUITE 900 WASHINGTON, DC 20004-2128			WEST, JEFFREY R	
			ART UNIT	PAPER NUMBER
			2857	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/051,297

Applicant(s)

WALTER ET AL.

Examiner

Jeffrey R. West

Art Unit

2857

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 January 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Claim Objections***

1. Claims 1, 10, 18, and 19 are objected to because of the following informalities:

In claim 1, line 11, to avoid problems of antecedent basis, "the electronic transducer" should be ---the electrical transducer---.

In claim 1, line 14, "path includes" should be ---path including---.

In claim 10, line 3, to avoid problems of antecedent basis, "the single quadrant amplifier" should be ---the single quadrant multiplier---.

In claim 18, line 1, to avoid problems of antecedent basis, "the duration" should be ---a duration---.

In claim 18, line 2, to avoid problems of antecedent basis, "the duration" should be ---a duration---.

In claim 19, line 1, to avoid problems of antecedent basis, "the duration" should be ---a duration---.

In claim 19, line 2, to avoid problems of antecedent basis, "the duration" should be ---a duration---.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 18 and 19 rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "much longer" in claims 18 and 19 is a relative term which renders the claim indefinite. The term "much" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention since "much longer" can refer to a wide variety of lengths of time depending on the specific application in the art.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 2, 5, 7, 9, 16, and 18-21, as may best be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over DE Patent No. 4016922 to Popp in view of U.S. Patent No. 5,416,723 to Zyl.

Popp discloses an electrical transducer using a two-wire process (001) comprising an analog sensor that detects a quantity to be measured (009, lines 2-6), an analog end stage which is connected downstream of the sensor at the output end of the transducer (010, lines 32-35 and "13" in Figure 1), a processor circuit (010, lines 26-27 and "7" in Figure 1), wherein the processor circuit is not connected

serially between the sensor and the analog end stage so that an analog measurement signal transmission path is realized (Figure 1), the analog end stage converting an output signal of the sensor into an impressed output current with a magnitude which is a measure of the quantity to be measured and is fixed within a range of about 0 to 20 mA, specifically about 4 to 20mA (010, lines 32-36 and Figure 1), the electrical transducer being controlled by the processor circuit (004, lines 1-8).

Popp discloses the analog measurement signal transmission path including an analog scaling unit ("6" in Figure 1), the output signal of the sensor and at least one analog setting value are supplied to the analog scaling unit (010, lines 1-8 and Figure 1), and the output signal of the analog scaling unit is supplied to the analog end stage (Figure 1).

Popp discloses that the analog scaling unit is an analog arithmetic circuit to which as the at least one analog setting value a DC voltage signal is delivered (010, lines 1-11) wherein the analog arithmetic circuit comprises at least one analog multiplier and at least one sign-evaluating (i.e. adding or subtracting) accumulator acting as an adder and/or subtractor (010, lines 11-19).

Popp discloses a power source that produces a non-zero output current (002, lines 14-16).

As noted above, the invention of Popp teaches many of the features of the claimed invention and while Popp does teach providing both an analog path and a digital path wherein the digital path includes a microprocessor that is not active during normal measurement operation but only provided to perform corrections (004,

lines 1-5), Popp does not explicitly disclose that the processor be shifted temporarily from an awake mode into a sleep mode in which the processor is inactive.

Zyl teaches a loop powered process control transmitter operating at a loop power of between 4 and 20 mA (column 1, lines 5-16) wherein during normal operation of the process control transmitter, the microprocessor circuit is shifted temporarily from an awake mode into a sleep mode in which the processor circuit is inactive (column 2, lines 20-30 and column 3, lines 14-18).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp to explicitly disclose that the processor be shifted temporarily from an awake mode into a sleep mode in which the processor is inactive, as taught by Zyl, because the invention of Popp does teach that the microprocessor is inactive during normal transducer operation and Zyl suggests that the combination would have improved the operation of the loop-powered transducer of Popp by complying with the strict power requirement of loop-powered devices (column 2, lines 13-30 and column 4, lines 37-56).

Further, with respect to claims 18 and 19, since the invention of Popp does teach providing both an analog path and a digital path wherein the digital path includes a microprocessor that is not active during normal measurement operation but only provided to perform corrections (i.e. the duration of the processor inactivity is much longer than the duration of the processor activity) and the invention of Zyl teaches that the microprocessor is shifted from an awake mode into a sleep mode, the

combination would have provided that the duration of the sleep mode of the processor circuit is much longer than the duration of the awake mode.

6. Claims 3, 4, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Popp in view of Zyl and further in view of U.S. Patent No. 5,886,565 to Yasui.

As noted above, the invention of Popp and Zyl teaches many of the features of the claimed invention including an analog scaling unit as an analog arithmetic circuit to which as at least one analog setting value a DC voltage signal is delivered from a microprocessor. The invention of Popp and Zyl, however, does not specify how this DC voltage is supplied.

Yasui teaches a reference voltage generating circuit having an integrator that generates a reference voltage using a voltage dividing circuit that divides a voltage supplied from a power source for use by the integrator (abstract).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp and Zyl to include an active integrator for generating the reference voltage, as taught by Yasui because Yasui suggests a corresponding circuit applicable and needed in the invention of Popp and Zyl in order to generate a reference voltage as well as assuring low power consumption and a stable output characteristic (column 1, lines 44-47).

Further, since the DC voltage signal of Popp and Zyl is generated by the microprocessor, the modification of Popp and Zyl with the control circuit integrator of

Yasui would provide an active integrator as part of a control circuit within the processing circuit.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Popp in view of Zyl and further in view of U.S. Patent No. 5,714,903 to Bruccoleri et al.

As noted above, the invention of Popp and Zyl teaches many of the features of the claimed invention and while the combination does teach an analog scaling unit including an analog multiplier, the combination does not specify that the multiplier be a single-quadrant multiplier.

Bruccoleri teaches a low-consumption analog multiplier that is a single-quadrant multiplier (column 4, line 66 to column 5, line 3).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp and Zyl to specify that the multiplier by a single-quadrant multiplier, as taught by Bruccoleri, because Bruccoleri suggests a corresponding multiplier for use in the invention of Popp and Zyl using a multiplier that would have improved efficiency by lowering current consumption while increasing error compensation (column 4, line 66 to column 5, line 3).

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Popp in view of Zyl and further in view of U.S. Patent No. 3,805,092 to Henson.

As noted above, the invention of Popp and Zyl teaches many of the features of the claimed invention and while the invention of Popp and Zyl does teach an analog



Art Unit: 2857

scaling circuit including an analog multiplier, the combination does not specify the makeup of the multiplier.

Henson teaches an electronic analog multiplier comprising a plurality of transistors (abstract) and a plurality of operational amplifiers (column 4, lines 32-38 and Figure 3).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp and Zyl to specify the makeup of the multiplier, as taught by Henson, because the combination would have provided a suitable multiplier for use in the invention of Popp and Zyl, that, as suggested by Henson, would have been suitably biased (column 4, lines 32-38) and operated at high operating speed without normally encountered errors caused by the high speed and/or transistor mismatch (column 2, lines 1-11).

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Popp in view of Zyl and Bruccoleri and further in view of U.S. Patent No. 6,057,794 to Takamuki.

As noted above, Popp in combination with Zyl and Bruccoleri teaches many of the features of the claimed invention and while the invention of Popp, Zyl and Bruccoleri, does include an analog scaling unit with an adder, subtractor, and single quadrant multiplier, and further while the combination does include an analog-digital converter as an input to the analog scaling unit, the combination does not specify the makeup of the analog-digital converter.

Takamuki teaches a sigma-delta modulation circuit as part of an analog-digital converter (column 1, lines 6-8) including an analog multiplier, adder, and subtractor (column 10, lines 5-14) with an adder connected through a delay circuit and a converter to the input of a multiplier and an adder and subtractor connected to the output of the multiplier (Figure 5).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp, Zyl, and Bruccoleri to specify that the analog-digital converter as an input to the analog scaling unit comprises an analog multiplier, adders, and subtractor, as taught by Takamuki, because while the invention of Popp, Zyl, and Bruccoleri is silent as to the makeup of the an analog-digital converter, Takamuki suggests a corresponding circuit applicable and necessary to implement the converter with improved operation through amplitude control using a small, simple configuration (column 2, lines 25-27).

Although the combination of Popp, Zyl, and Bruccoleri provides an analog-digital converter electrically coupled to the analog scaling circuit rather than part of the analog scaling circuit itself, it would have been obvious to one having ordinary skill in the art to provide the A/D converter, and corresponding sigma-delta circuit with multiplier, adders, and subtractor, and the analog scaling circuit as one circuit in order to adhere to space constraints. Further, it has been held that forming in one piece which has formerly been formed in two pieces and put together involves only routine skill in the art (see *Howard v. Detroit Stove Works*, 150 U.S. 164 (1893)).

10. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Popp in view of Zyl and further in view of U.S. Patent No. 5,207,101 to Haynes.

As noted above, the invention of Popp and Zyl teaches many of the features of the claimed invention and while the invention of Popp and Zyl does teach a circuit connected between the analog scaling unit and the analog end stage for attenuating the sensed signal by performing an average calculation, wherein the attenuating circuit comprises an RC element (Popp, 011, lines 5-20), the combination does not include the specifics of the circuit, specifically, regarding an adjustable time constant.

Haynes discloses a two-wire ultrasonic transmitter comprising a sensor that detects a quantity to be measured (column 2, lines 19-22), an analog end stage, comprising an amplifier circuit, connected downstream of the sensor (Figure 4b, "52"), a processor circuit, including a processor and drive circuit (column 7, lines 41-42) and an analog measurement signal transmission path (see subsequent circuitry from X1 in Figure 4a), the analog end stage including, between the analog scaling unit and the subsequent analog end stage circuitry, an attenuator comprising an RC element (column 2, lines 58-60 and column 8, lines 52-64), having an adjustable time constant (i.e. adjustable resistor and capacitor values) wherein an error output of the attenuator can be compensate by a control circuit (i.e. comparator with threshold detection) (column 8, line 65 to column 9, line 9).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp and Zyl to include the specifics of the attenuating circuit,

specifically, regarding an adjustable time constant, as taught by Haynes, because the combination would have provided improved the transducer operation by allowing modification of the attenuating circuit as desired while, as suggested by Haynes, improving the performance of the transducer of Popp and Zyl by effectively minimizing dead band (column 8, lines 52-64).

11. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Popp in view of Zyl and further in view of U.S. Patent No. 5,252,967 to Brennan et al.

As noted above, the invention of Popp and Zyl teaches many of the features of the claimed invention and while the invention of Popp and Zyl teaches operation in two-wire mode, the combination does not disclose means for operation in three-wire mode.

Brennan teaches a reader/programmer for two and three wire utility data communications systems including three power supply terminals (i.e. receptacles) (column 6, lines 18-25) wherein upon automatic detection of a predetermined voltage of an interrogation signal at the terminals (column 7, lines 43-55 and column 9, lines 47-49), the measurement device sends a wake-up signal to its microprocessor (column 10, lines 30-37) and based upon the interrogation signal, which powers the device (column 9, lines 26-31), operates in either two or three wire mode (column 9, line 50 to column 10, line 10).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp and Zyl to include means for operation in three-wire mode, as taught by Brennan, because Popp and Zyl teaches a transmitter for use in pressure measurement and, as suggested by Brennan, the combination would have provided means for a utility meter, such as a pressure or flow meter, to be used in two or three wire modes thereby increasing the versatility of the device while reducing the burden on the user (column 2, lines 7-32).

### ***Response to Arguments***

12. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

13. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

U.S. Patent No. 4,524,624 to Di Noia et al. teaches a pressure and differential pressure detector and transmitter for use in hostile environments including a detector arrangement comprising an adder, subtractor, and multiplier.

U.S. Patent No. 5,956,663 to Eryurek teaches a signal processing technique which separates signal components in a sensor for sensor diagnostics.

U.S. Patent No. 5,083,091 to Frick et al. teaches a charge balanced feedback measurement circuit.

JP Patent Application Publication No. 04-359399 to Tamura et al. teaches a three-wire signal processor that converts a three-wire signal into a two-wire signal.

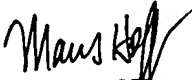
U.S. Patent No. 3,948,098 to Richardson et al. teaches a vortex flow meter transmitter that can be used in two-wire or three-wire operation.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone number for the organization where this application or proceeding is assigned is (703)308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw  
September 5, 2005

  
MARC S. HOFF  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800